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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,070	11/20/2003	Hendrik F. Hamann	YOR920030368US1 (8728-643	8659

46069 7590 04/16/2008

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EXAMINER	
GEORGE, PATRICIA ANN	

ART UNIT	PAPER NUMBER
1794	

MAIL DATE	DELIVERY MODE
04/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/718,070	HAMANN ET AL.	
	Examiner	Art Unit	
	Patricia A. George	1794	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,8-13,22,23,26,27 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,8-13,22,23 and 26-27, and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/6/2008 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3, 4, 5, 8, 11, 12, 13, 22, 23 and 26-27, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6,927,410), in view of Lowrey et al (6,943,365) (herein referred to as Lowrey) and Ovshinsky et al. (2003/0212724). Seo et al. (Investigation of Crystallization Behavior of Sputter-Deposited Nitrogen-Doped

Amorphous $Ge_2Sb_2Te_5$ Thin Films; Jpn. J. Appl. Phys. Vol.39 (2000) 745-751; Part 1, No. 2B, 28 February 2000) provides evidence in support of the rejection below.

Chen teaches: a multi-bit phase changing memory device (ab.), including: layers of phase change material (ab.) separated by layers of conductive interface (ab.), produced with varying degrees of resistivity (col.2, l.27).

Chen teach a multi-bit phase change memory cell (claim1) or multi-bit phase change memory (claim 22), where each of said plurality of phase change material layers has a different height from one another, please refer to: column 1, lines 35 through column 2, lines 36, where Chen teaches phase change memory devices, such as multi-bit memory cells, i.e. multi-bit phase change memory cell (claim 1) and i.e. multi-bit phase change memory (claim 22); and see column 8, lines 28-36, where Chen teaches a plurality of phase change material layer with different thicknesses, i.e. where plurality of phase change material layers has a different height from one another. The term thickness is interpreted as a dimension between two surfaces, as opposed to length or width, i.e. used to describe the height of a semiconductor layer.

Although Chen describes the thickness of the phase change material layers may be different from one another, Chen is silent to the height increasing while surface area decrease, of each of the phase change materials along a direction from the first outer conductor layer to the second outer conductive layer, as in claim 1.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to select any desired height and surface area, of each of the phase change materials along a direction from the first outer conductor layer to the second

outer conductive layer, as in applicants' claimed limitation, when forming the multi-bit phase changing memory device, as Chen, because Chen teaches it is effective to provide phase change material layers of varying thickness that are different from one another. In the absence of unexpected results, one of ordinary skill would form the phase change layers as desires, including applicants' specifically claimed height increasing while surface area decrease, of each of the phase change materials along a direction from the first outer conductor layer to the second outer conductive layer, because the reference does not limit the ordered configuration of phase change materials.

Further, because Chen discloses a plurality of phase change material layers with different thicknesses, see column 8, lines 28-36, one of ordinary skill in the art would recognize that the plurality of phase change material layers with different thicknesses, as in the reference of Chen, would also have different surface areas from one another, because the mathematical equation for surface area is dependent on height (i.e. thickness) as a multiplier, and a variety of heights would calculate a result with a variety of surface areas. Applicants' have not shown anything unexpected when forming the claimed ordered configuration of phase change materials.

Chen teaches when the chalcogenide material (i.e. phase change material) is known to be programmed between an amorphous state that exhibits a relatively high resistivity, and a crystalline state that exhibits a relatively low resistivity, wherein the high and low resistivities represent programmed bit values of "1" and "0", which can be

sensed by then measuring the resistivity of the chalcogenide material, which is written on the multi-bit phase change memory cell is adapted such that when each of the plurality of phase change material layers are in an amorphous state then each of the plurality of phase change material layers each have similar resistivity.

Chen fails to be explicit about the phase change material layers in an amorphous state having the same resistivity, as in claim 3.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the method of forming a multi-bit phase changing memory device, of Chen, to include when the phase change material layers are in an amorphous state each of the plurality of phase change material layers have the same resistivity, As applicants' limitation, because Chen teaches when the phase change material layers are in an amorphous state each of the plurality of phase change material layers have a similar resistivity.

Chen does not teach the structure of the first and second conductive layers, disposed on opposite sides of the memory cell, as in claim 1.

Lowrey illustrates the first outer conductive layer (130a) disposed at the right side (i.e. one side) of the memory cell and a second outer conductive layer (130b) disposed at the left side (i.e. a side opposite to the one side) of the memory cell, in figure 1A, and refers to this configuration as the “rapier” design of conductor spacer.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the structure of the first and second conductive layers,

disposed on opposite sides of the memory cell, as in Lowrey, when forming the multi-bit phase changing memory device, of Chen, because Lowrey teaches this configuration is an improvement as it reduces the size of the area of contact of the memory material, thereby reducing the total current needed to program the memory device.

As to the limitation wherein each of the plurality of phase change material layers have the same resistivity, Chen teaches phase change memory devices use memory materials that are electrically switched (programmed) between different structured states that exhibit different electrical read-out properties. For example, memory devices are programmed between a generally amorphous state that exhibits a relatively high resistivity, and a generally crystalline state that exhibits a relatively low resistivity. The phase change material is programmed by heating the material, whereby the amplitude and duration of the heating dictates whether the phase change material is left in an amorphous or crystallized state. The high and low resistivities represent programmed bit values of "1" and "0", which can be sensed by then measuring the resistivity of the phase change material, which is written on plurality of phase change material layers have the same resistivity (see background, lines 35-52). Chen further teaches first a high current pulse is passed through the memory device to generate a thermal pulse that amorphousizes *all* of the phase change material layers. Then a crystallizing thermal pulse creates a temperature gradient across the memory material, where the various layers are *asymmetrically* heated (i.e. top layers hotter than bottom layers). Over the duration of the crystallizing thermal pulse, the various layers of phase change

materials are sequentially crystallized, top down, one layer at a time, which is also written on plurality of phase change material layers have the same resistivity.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, that the programmed bit vaulues of “1” and “0” represent high and low resistivities, which can be sensed by then measuring the resistivity of the phase change material; that the step which includes a high current pulse, resets all the phase change material layers, preparing them to be programmed with a thermal pulse; and when the high current pulse resets all the phase change material layers they have the same programming value and the same resistivity.

Further on the same topic, Seo et al. provides evidence that nitrogen doping (i.e. implanting) of the Ge2Sb2Te5 phase-change films allows the crystalline process to occur in a primary nucleation step, an improved stability of the amorphous phase.

Although, Chen fails to explicitly teach implanting the Ge2Sb2Te5 has an effect on the resistivity of the mater, however it would have been obvious to one of ordinary skill in the art at the time of invention was made, that an improvement to the stability of the amorphous phase of Ge2Sb2Te5 that allows the crystalline process to occur in one primary nucleation step, as Seo, would greatly impact the resistivity of the film because it would allow for a change to the state of the resistance to occur more rapidly and remain fixed in that state until another change is desired, therefor allowing all the phase change material layers to be more responsive to holding the same value of resistivity

when programmed as less device failure occurs, clearly an improvement in manufacturing.

The modified teaching of Chen is silent as to the electrical resistance of each of the plurality of phase change material layers increasing from the 1st outer conductive layer to the 2nd outer conductive layer.

As for the electrical resistance of each of the plurality of phase change material layers increasing from the 1st outer conductive layer to the 2nd outer conductive layer, Ovshinsky teaches the electrical resistance of a phase change layer is determined by the amount of energy applied (i.e. a result effective variable). See para. 32-33.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the method of forming a device with phase change layers, as Chen, to include electrical resistance of each of the plurality of phase change material layers increasing from the 1st outer conductive layer to the 2nd outer conductive layer, as applicants' claimed limitation, because Ovshinsky teaches the electrical resistance of a phase change layer is determined by the amount of energy applied (i.e. a result effective variable), and therefore it would have been obvious to one with skill in the art at the time of the invention to determine the optimal value for electrical resistance used in the process by modifiying the amount of energy applied through routine experimentation to acchive any desired results, including applicants' each of the plurality of phase change material layers increasing from the 1st outer conductive layer to the 2nd outer conductive layer.

As for claim 4, Chen's figures 4A-G illustrate wherein each of the plurality of phase change material layers have a different phase transition temperature, also concealed in column 5, lines 23-26.

As for claim 5, Chen explains a method for operating a phase change memory having a volume of memory material, including a plurality of discrete layers of materials. The method includes applying heat to the volume of material for a predetermined amount of time (col.3, l.28-43), which demonstrates the following limitation claimed: each of the plurality of phase change material layers has the same phase transition temperature.

As for claim 8, Ovshinsky illustrates all the limitations of claim 8 in figure 3, and explained in Example 1: a dielectric layer (60) formed between the first outer electrode (90) and the second outer electrode (30) and along sides of at least one other conductive layer (70) and a phase change material layer (80) disposed directly adjacent to the at least one other conductive layer (110).

As for claim 11, Chen discloses the phase change material layers are made of Ge.sub.2Sb.sub.2Te.sub.5 (col.4, l.52).

As for claim 12, Chen discloses the plurality of conductive layers are made of W, TiW, etc. (col.4, l.44).

As for claim 13, Chen demonstrates the number of phase change material layers corresponds to the number of possible bit values storable (col.4, l. 36-38).

As for claim 22, Chen expresses memory technologies can be read only, write once only, or repeatedly read/write which represents a programming circuit that writes

data to the array of multi-bit phase change memory cells; and a sensing circuit that reads out data from the array of multi-bit phase change memory cells. All other limitations of claim 22 are discussed above.

As for claim 23, see discussion to claim 11.

With respect to claims 26-27, and 29, all limitations have been previously presented, and therefor are discussed in the rejection above.

Claim Rejections - 35 USC § 103

Claims 6, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, Lowrey, and Ovshinsky et al. (evidenced by Hun Seo et al.), as applied to claims 1, 4, 5, 11, 12, 13, 22, 23 and 26-27, and 29 above, further in view of Klersy et al. (5,536,947).

The modified teaching of Chen fails to demonstrate the plurality of phase change material layers are of similar resistivity (as in applicants' claim 3), and are made of the same or different material (as in claims 9 and 10).

Klersy et al. teaches compositional modification of phase change materials, including use of any means to modifying the compositions, such as modifying: the volume to yield stable values of resistance, which points to the plurality of phase change material layers having different dimensions (as in applicants' claim 6); and the phase change material layers made of the same or different material, as in claims 9 and 10 (col.14, l.3-54).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the method of forming phase change materials, as the

modified teaching of Chen, to include the plurality of phase change material layers are of similar resistivity, and are made of the same or different material, as in claims 3, 6, 9 and 10, because Klersey teaches compositional modification of phase change materials, including use of any means to modifying the compositions.

Response to Arguments

Applicants' argue, on pages 8-11, that the previous office actions fail to address the newly amended limitations toward resistivity and electrical resistance properties now recited in amended claims 1, 22 and 26. Examiner agrees. Please see the new grounds for rejections offered above. Rejections of all other limitations, not argued, are deemed proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571) 272-5955. The examiner can normally be reached on Tue. - Fri. between 9:00 am and 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Keith Hendricks can be reached on (571) 272-1401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Patricia A George
Examiner
Art Unit 1794

04/01/08
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